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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,749	SCHRADER ET AL.	
	Examiner	Art Unit	
	IAN N. MOORE	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In response to Appeal Brief

1. In view of the appeal brief filed on 4/16/09, PROSECUTION IS HEREBY REOPENED. The new grounds of rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Derrick W Ferris/

Supervisory Patent Examiner, Art Unit 2416

Response to Arguments

2. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-13 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kichise (WO 00/62254) in view of Ochi (U.S. 5,299,003).

Regarding Claim 1, Kichise discloses an apparatus (see FIG. 2, voice processor 2) for the transmission of time-synchronous multi-media data (see FIG. 2, transmission of voice/video/MPEG data, which is time-synchronous multi-media data; see page 2, paragraph 28; see page 3, paragraph 45; see page 4, paragraph 51) from a sender (FIG. 2, 3, transmitter line interface 3) to a receiver (FIG. 2, IP network interface 4) using a IP network (FIG. 2, using IP network; note that a network of digital signal processing units 5 process IP packets, thus it is a IP network; see page 2, paragraph 28-29), wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver (see FIG. 2, the voice/video/MPEG data is processed at line interface 3 and IP network interface; see page 2, paragraph 25-32), comprising:

the sender receiving time-synchronous multi-media data (FIG. 2, line interface 3 receives voice/video/MPEG data, which is time-synchronous multi-media data; see page 2, paragraph 28-31);

a mechanism (FIG. 2, 3, digital signal processing unit 5) connected to said sender for processing the time synchronous multi-media data for output to said IP network (FIG. 2, 3,

connection to line interface 3 for processing voice/video/MPEG data for transmitting/output to IP network; see page 2-3, paragraph 29-33)

the receiver connected to said IP network for receiving processed time-synchronous multi-media data transmitted over said IP network (FIG. 2, 3, IP network interface 4 connected to IP network for receiving packetized/processed voice/video/MPEG data over IP network; see page 2-3, paragraph 29-33)

said mechanism (FIG. 3, digital signal processing unit 5) comprising:

a first processing unit (FIG. 3, 5, data converter (DSP) 11) composed of multiple subcomponents (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b)) and a RTP out 26 which outputs IP packets from digital encoded signal (i.e. IP packetizer); see page 3-4, paragraph 43-47), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 5, a combined ENC-DEC 25a-b and RTP out 26 designed/configured process audio/video/MPEG data in specific/particular and different/dissimilar way/method; see page 3-4, last paragraph 44-51), a plurality of said multiple subcomponents being selected from the group consisting of a codec (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b); see page 3-4, paragraph 43-47) and an IP packetizer (FIG. 5, RTP out 26 which packetized the audio/video/MPEG signal into VoIP packets; see page 3-4, last paragraph 44-51);

a second processing unit parallel to the first processing unit (FIG. 3, 5, data converter (DSP) 12 parallel to data converter (DSP) 12)), composed of multiple subcomponents (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b)) and a RTP out 26 which outputs IP packets from digital encoded signal (i.e. IP packetizer); see page 3-4,

paragraph 43-47), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 5, a combined ENC-DEC 25a-b and RTP out 26 designed/configured process audio/video/MPEG data in specific/particular and different/dissimilar way/method; see page 3-4, last paragraph 44-51), a plurality of said multiple subcomponents being selected from the group consisting of a codec (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b); see page 3-4, paragraph 43-47) and an IP packetizer (FIG. 5, RTP out 26 which packetized the audio/video/MPEG signal into VoIP packets; see page 3-4, last paragraph 44-51);

wherein the subcomponents of second processing unit are setup and adapted based on changed sender network characteristics (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b) and RTP out 26 are set/configured and changed/adapted according to changed/adapted line input network characteristics such as coding characteristics (G.7231, G.729, G.711), frequency modulation characteristics of FMD 22, and echo cancellation characteristic echo canceller 23; see page 3, paragraph 44-46);

wherein data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit (FIG. 3; processing and transmission of audio/video/MPEG data is continued/parallel-processed in the data converter 11 while data converter 12 is setup and fit/adapted for parallel processing; see page 2-3, paragraph 33-35, 45-46); and

a switch selecting between the first and second processing units (see FIG. 3, layer 4 switch 16 switching/changing/selecting data converter (DSP) 11 and data converter 12; see page 3, paragraph 38-42), the processing and transmission of the time-synchronous multi-media data

initially being performed by the first processing unit (see FIG. 3, processing and transmission of audio/video/MPEG data primarily/initially performed by the converter 11; see page 3, paragraph 38-42), the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit (see FIG. 3, processing and transmission of audio/video/MPEG data primarily/initially performed by the converter 12; see page 3, paragraph 38-42) such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit (see FIG. 3, 5, the processing and transmission of audio/video/MPEG is processed within the converter 12; see page 2-3, paragraph 31-46), the output of said switch being connected to said IP network (see FIG. 3, 5, the output/transmitting of the layer 4 switch is connected to the IP network; see page 3, paragraph 35-42).

Although Kichise discloses "a switch selecting between the first and second processing unit, the processing and transmission is initially being performed by the first processing unit and the processing and transmission is performed using the second processing unit" as set forth above,

Kichise does not explicitly disclose "*after switching by the switch*".

Ochi discloses a switch (see FIG. 1, Switch circuit 18) selecting between the first and second processing units (see FIG. 1, switching/changing/selecting between the combined system of first memory 12, transmitter 14 and third memory 16, and the combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 6-55), the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit (see FIG. 1, 2a-h, processing and transmission of video/ multi-media primarily/initially performed by the combined system of first memory 12, transmitter 14 and

third memory 16 at t0 to t1, t2 to t3, and t4 to t5) and after switching, the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit (see FIG. 1, 2a-h, after switching processing and transmission of video/ multi-media data signal is processed by the combined system of second memory 13, transmitter 15 and fourth memory 17 at t1 to t2, t3 to t4, and t5 to t6) such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit (see FIG. 1, 2a-h, such that the processing and transmission of vide/ multi-media data signal is performed by the combined system of second memory 13, transmitter 15 and fourth memory 17); see col. 6, line 26 to col. 7, line 10), the output of said switch being connected to said network (see FIG. 1, the output of switch 18 is connected to the network; see col. 6, line 26 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*after switching by the switch*", as taught by Ochi in the system of Kichise, so that it would provide allow a signal to pass through a transmission circuit in positive time frequency and the all the signal to be transmitted through another transmission circuit; see Ochi col. 2, line 25-46.

Regarding Claim 2, Kichise discloses wherein the setup and adaptation of the second processing is started using a trigger event (FIG. 1, configuration/setting-up and changing/adaptation of the converter 12 is stared using the activating/triggering event/result; see page 3, paragraph 38-45). Ochi also discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 3a-j, the configuration/setting-up and fitting/adaptation of a combined system of second memory 13, transmitter 15 and fourth memory 17 is began/stated using waveform up/down event; see col. 6, line 26 to col. 7, line 10).

Regarding Claim 3, Kichise discloses wherein the switching is performed after the completion of the setup and adaptation of the second processing unit (FIG. 3, 5, switching by layer 4 switch is performed after switch after completion/ending of setup/configuration/setting of converter 12; page 3, paragraph 38-45). Ochi also discloses wherein the switching is performed after the completion of the setup and adaptation of the second processing unit (see FIG. 1, switching is performed after completion/ending of setup/configuration/setting and adaptation/fitting of the combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 6-55).

Regarding Claim 4, Kichise discloses wherein the switching is performed after reaching a certain switching condition (FIG. 3, Layer 4 switching is performed after reaching the condition of reaching/analyzing and determining the incoming IP traffic; see page 3, paragraph 38-39). Also, Ochi discloses wherein the switching is performed after reaching a certain switching condition (see FIG. 2, switching is performed after reaching t1, t3, and/or t5 (i.e. condition) which triggers switching; see col. 6, line 6-55).

Regarding Claim 5, Kichise discloses certain switching condition as set forth above.

Kichise does not explicitly disclose "at least one given parameter reaches at a predetermined value".

However, Ochi discloses the certain switching condition is whether at least one given parameter reaches at a predetermined value (see FIG. 2, switching condition is whether the time reaching t1, t3, and/or t5; see col. 6, line 6-55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*at least one given parameter reaches at a predetermined*

value", as taught by Ochi in the system of Kichise, so that it would provide allow a signal to pass through a transmission circuit in positive time frequency and the all the signal to be transmitted through another transmission circuit; see Ochi col. 2, line 25-46.

Regarding Claim 6, Kichise discloses wherein the time-synchronous multi-media data is processed in the first processing unit using a plurality of said multiple subcomponents (see FIG. 5, audio/video/MPEG data is processed in the converter 11 using a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b)) and a RTP out 26 which outputs IP packets from digital encoded signal (i.e. IP packetizer); see page 3-4, paragraph 43-47). Also, Ochi discloses wherein the time-synchronous multi-media data is processed in the first processing unit using a plurality of said multiple subcomponents (see FIG. 1, **video/ multi-media** data is processed in the a combined system comprising first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 7, Kichise discloses wherein the subcomponents includes at least one of a codec, a packetizer (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b); see page 3-4, paragraph 43-47; RTP out 26 which packetized the audio/video/MPEG signal into VoIP packets; see page 3-4, last paragraph 44-51). Also, Ochi discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 1, a combined processing system comprising first memory 12 or third memory 16; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 8, Ochi discloses wherein the time-synchronous multi-media data is processed in the second processing unit using a plurality of said multiple subcomponents (see FIG. 5, audio/video/MPEG data is processed in the converter 12 using a combination of encoder

ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b); see page 3-4, paragraph 43-47; RTP out 26 which packetized the audio/video/MPEG signal into VoIP packets; see page 3-4, last paragraph 44-51). Also, Ochi discloses wherein the time-synchronous multi-media data is processed in the second processing unit using a plurality of said multiple subcomponents (see FIG. 1, a video/ multi-media data is processed in a combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 9, Kichise discloses wherein the subcomponents includes at least one of a codec and a packetizer (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b); see page 3-4, paragraph 43-47; RTP out 26 which packetized the audio/video/MPEG signal into VoIP packets; see page 3-4, last paragraph 44-51). Also, Ochi discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 1, a combined processing system comprising second memory 13 or fourth memory 17; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 10, Kichise discloses wherein the subcomponents are connected during the setup (see FIG. 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b); see page 3-4, paragraph 43-47; RTP out 26 which packetized the audio/video/MPEG signal into VoIP packets are connected during the configuration/setups; see page 3-4, last paragraph 44-51). Also, Ochi discloses wherein the subcomponents are connected during the setup (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 are connected during the configuration/setups; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 11, Kichise discloses wherein the first and second processing unit is initialized after the setup (FIG. 3, 5, converter 11 and 12 are /started/begin processing after the

configuring/setting-up; see page 3, paragraph 33-35). Ochi discloses wherein the first and second processing unit is initialized after the setup (see FIG. 1, a combined system of first memory 12, transmitter 14 and third memory 16, and a combined system of second memory 13, transmitter 15 and fourth memory 17 are initialized/started/begin processing after the configuring/setting-up; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 12, Kichise discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (FIG. 3, 5, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b)) and a RTP out 26 which outputs IP packets from digital encoded signal (i.e. IP packetizer) of parallel to data converter (DSP) 12 (of converter 12) is adapted/fit/adjust/corresponds to a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b)) and a RTP out 26 which outputs IP packets from digital encoded signal (i.e. IP packetizer) (of converter 13); see page 3-4, paragraph 43-47). Also, Ochi discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (see FIG. 2, each second memory 13, transmitter 15 or fourth memory 17 is adapted/fit/adjust/corresponds to other second memory 13, transmitter 15 or fourth memory 17; or other first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 26), or the changed data rate, or changed network characteristics (changing/switching data rate or network transmission characteristic; see col. 5, line 55 to col. 6, line 55).

Regarding Claim 13, Kichise does not explicitly disclose "*after the switching process, the subcomponents of the first processing unit are de-attached from each other*".

Ochi discloses wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other (see FIG. 1, after switching, first memory 12,

transmitter 14 and third memory 16 are separated/de-attached from second memory 13, transmitter 15 or fourth memory 17; see col. 5, line 55 to col. 6, line 55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*after the switching process, the subcomponents of the first processing unit are de-attached from each other*", as taught by Ochi in the system of Kichise, so that it would provide allow a signal to pass through a transmission circuit in positive time frequency and the all the signal to be transmitted through another transmission circuit; see Ochi col. 2, line 25-46.

Regarding Claim 15, Kichise discloses wherein after switching by the switch (FIG. 3, after switching by the layer 4 switch 16), the subcomponents of the first processing unit remain connected (FIG. 3, a combination of encoder ENC 25a and decoder DEC 25b (i.e. CODEC 25a-b)) and a RTP out 26 which outputs IP packets from digital encoded signal (i.e. IP packetizer) of converter 11 are still connected; see page 3, paragraph 38-42). Ochi discloses wherein after switching by the switch, the subcomponents of the first processing unit remain connected (see FIG. 1, after switching memory 12, transmitter 14 and third memory 16 are still connected; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 16, Kichise discloses wherein a plurality of second processing unit are setup (FIG. 3, converters 12 and 13 are configured/setup; see page 2-3, paragraph 43-46).

Kichise does not explicitly discloses "*adapted on changed data rate and network characteristics*".

Ochi discloses wherein a second processing unit (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 are configured/setup, and after

switching by the switch; see col. 5, line 55 to col. 6, line 55) are setup and adapted based on changed data rate and network characteristics (see FIG. 2a-h, setup/configured and fit/adapted for parallel storage and processing according to transmitting/sending data rate and network transmission characteristic; see col. 5, line 55 to col. 6, line 55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*adapted on changed data rate and network characteristics*", as taught by Ochi in the system of Kichise, so that it would provide allow a signal to pass through a transmission circuit in positive time frequency and the all the signal to be transmitted through another transmission circuit; see Ochi col. 2, line 25-46.

Regarding Claim 17, Kichise discloses the additional processing unit (FIG. 5, converter 13) for processing and transmission of time-synchronous multi-media data (FIG. 5, for processing of audio/video/MPEG data) is used in sequence with the first and second processing units (FIG. 5, is used in parallel sequence with converter 11 and 12; see page 2-3, paragraph 35-45). Also, Ochi discloses the processing and transmission of time-synchronous multi-media data is used in sequence with the first and second processing units (see FIG. 2, a combined system of memory 12, transmitter 14 and memory 16 process the **video/ multi-media** data (i.e. processing of video) in parallel sequence with second combined system memory 13, transmitter 15, memory 17; see col. 5, line 55 to col. 6, line 55).

Regarding Claim 18, Kichise discloses wherein the time-synchronous multi-media data is gathered with one of mechanisms for acquiring visual data and speech data (FIG. 2, 3, audio/video/MPEG data is collected/received by voice processor 2 for obtaining/acquiring image, voice and video data; see page 2, paragraph 28; see page 3, paragraph 45; see page 4,

paragraph 51). Also, Ochi discloses wherein the time-synchronous multi-media data is gathered with one of mechanisms for acquiring visual data and speech data (see FIG. 1; video data is collected/received by a apparatus for obtaining/acquiring video/ **multi-media** data (i.e. image/visual data and audio/speech data); see col. 5, line 55 to col. 6, line 26).

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kichise in view of Ochi (U.S. 5,299,003) further in view of Sastry (US006694373B1).

Regarding Claim 14, Kichise discloses the plurality of the second processing units is setup (FIG. 3, data converter 12 and 13 are configured/setup) and, after switching by the switch (FIG. 3, after switching by the switch 16; see page 2-3, paragraph 35-40). Ochi discloses the second processing units is setup and after switching by the switch (see FIG. 1, second memory 13, transmitter 15 or fourth memory 17 are configured/setup, and after switching by the switch; see col. 5, line 55 to col. 6, line 55); and the subcomponents of the first processing unit (see FIG. 1, second memory 13, transmitter 15 or fourth memory 17) as set forth above in claim 1.

Neither Kichise nor Ochi explicitly disclose "the subcomponents of the first processing unit are included in one of the second processing units".

Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed) and after switching by the switch after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units (see FIG. 8, after switching by a switch 420/620, subcomponent 2 ADPCM (Adaptive Pulse Code Modulation for voice compressing) from DSP 801 (i.e. first processing unit) are now included in the DSP 803; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "the subcomponents of the first processing unit are included in one of the second processing units", as taught by Sastry in the combiend system of Kichise and Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick W. Ferris can be reached on 571-272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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